Revista Brasileira de Aplicações de Vácuo, v. 24, n. 2, 117-120, 2005.

EFFECT OF THE THERMAL SINTERING ON THE REAL CONTACT RESISTIVITY OF Al/N^+P AND Al/$TiSi_2$/N^+P STRUCTURES

R. Pestana*; S.G. Santos Filho
University of São Paulo – LSI/PSI/EPUSP
Av. Prof. Luciano Gualberto, 158 – Trav. 3, 05508-900, São Paulo, SP, Brazil

Received: July 25, 2005; Revised: November 23, 2005

Keywords: sintering, contact resistivity, current crowding.

ABSTRACT

The real contact resistivity parameter was investigated based on measurements using a cross-bridge Kelvin resistor for several recipes of thermal sintering. Using a computer program developed in MATLAB and based on a well-known three-dimensional multi-nodal resistor network, the Al/Si(N^+P) and Al/$TiSi_2$/Si(N^+P) structures were analyzed after sintering at temperatures of 420 and 435 °C during 30 minutes in forming gas. For sintering at 420 °C, it was noteworthy to observe high contact resistivity for the Al/$TiSi_2$/Si(N^+P) structure and differences up to 55% between real and apparent contact resistivities. However, after sintering at 435 °C, the Al/$TiSi_2$/Si(N^+P) structure presented a low contact resistivity of 7.2 $\mu\Omega cm^2$ while the Al/Si(N^+P) structure, in spite of presenting the lowest value of contact resistivity, also showed prohibitive high values of reverse leakage current after sintering at 435°C or 450°C.

1. INTRODUCTION

Fabrication of reliable low-resistance ohmic contacts and methods for accurate determination of the real contact resistivity (ρ_c), are important in the current integrated circuit production methods and their electrical characterization. It is known that the contact resistance can degrade the final electrical behavior of MOS field effect transistors and bipolar junction transistors [1-5].
Measurement procedures based on the cross-bridge Kelvin resistor have been used. However, parasitic factors may strongly affect the measurement accuracy for contact resistivity in the range of 10^{-6} to 10^{-7} Ωcm^2. In this paper, it is shown the results of a computer program developed in MATLAB, based on a three-dimensional multi-nodal resistor network, in which the lateral current crowding effect on the contact resistance parameter is determined as a function of the contact resistivity, sheet resistance of the diffused layer, and geometrical characteristics of the cross-bridge Kelvin resistor [5-9]. The real contact resistivity was obtained for Al/$TiSi_2$/Si(N^+P) and Al/Si(N^+P) structures for several thermal sintering conditions.
Sintering is a coalescence mechanism involving islands in contact with each other. Some authors [10] have shown the influence of time and temperature on the sintering, within tenths of a second where a neck is formed between islands and then successively thickens as atoms are transported into the region. The driving force for neck growth is simply the natural tendency to reduce the total surface energy (or area) of the system. Since the algebraic magnitude of mobility for atoms on convex island surfaces exceeds that for atoms situated in the concave neck, an effective concentration gradient develops between these regions. Variations in island surface curvature also increase local concentration differences that are alleviated by mass flow [10].
The appropriate choice of the thermal sintering conditions can collaborate to obtain low-resistance ohmic contacts for Al/Si(N^+P) and Al/$TiSi_2$/Si(N^+P) structures, as will be shown in this work.

2. MODELING

Besides the intrinsic resistance of a given material, when two different conductive materials are put in contact (for example, metal and semiconductor), the outcome is an additional resistance due to the contact itself; this resistance is known as contact resistance (Rc) [11]. This resistance occurs due to differences of work functions or surface states in a shallow layer at the semiconductor below the metal or due to a resistive material layer between metal and semiconductor that is prejudicial to a good contact.
Assuming the contact resistance as a relation between voltage and current, ρ_c* is defined as the apparent contact resistivity determined as the contact resistance multiplied by the contact area as follows [11]:

$$R_c = \frac{V}{I} = \frac{\rho_c^*}{A} \quad \textbf{(1)}$$

Where: A = contact area
V = total voltage drop across the contact
I = total current flowing in contact

This assumes a punctual model that does not work well if the lateral current crowding effect is significant. As the specific resistivity of the metal is always much smaller than that of the semiconductor, the electric current is not uniformly

* ricardo_pestana@br.schindler.com

distributed through the contact structure. Most of the current density flows through the smallest possible distance inside the semiconductor and then it passes to the metal [11,12]. Therefore, the use of the equation (1) can produce substantial error on the contact-resistivity determination for non-punctual models.

A computer program was developed in MATLAB Language Version 6.0.0.88 Release 12 in order to obtain the real contact resistivity, based on a well-known three-dimensional multi-nodal resistor network [5]. At first, based on a cross-bridge Kelvin resistor as shown in figure 1, it generates nodal conductance matrices, which depend on the sheet resistance of the diffused layer outside the contact region (Rsh), the sheet resistance of the diffused layer underneath the contact region (Rsk), the value of electric current applied during the test (I), the voltage drop across the contact and the geometric dimensions of the contact as shown in figure 2.

The distinction between the semiconductor layers outside and underneath the contact is often required for an accurate determination of the contact resistivity, since metallurgical reactions occurring in the contact preparation process may lead to appreciable modifications in the value of the sheet resistance underneath the contact [12]. Measurements with the electrostatic force microscope (EFM) have shown difference between sheet resistances, outside and underneath the ohmic contact. The accuracy on the determination of the sheet resistance is less than ±3% [13]. The program inputs are the diffused region width (DW), the diffused region length (DL), the contact width (CW), the contact length (CL), the track width (TW), the track length (TL), the distance among nodes (Δx), the value of Rsh, the value of Rsk, the applied current (I), the voltage on the contact (Vc) and the voltage on the track end (Vt).

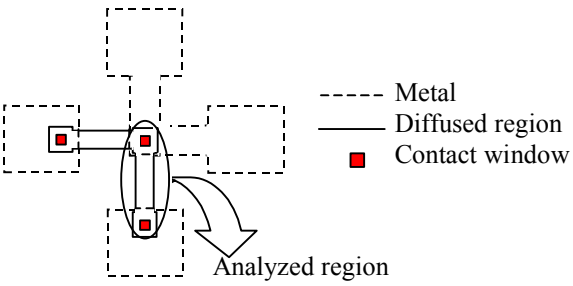

Figure 1 - Cross-bridge Kelvin resistor.

The analyzed region has been divided in cubic cells, Δx in length. For each cell, it was done a description of its resistive behavior by resistors R_1, R_2 and R_3 [5, 6] as shown in figure 3, where:

$$R_1 = \frac{R_{sh}}{2} \quad (2)$$

$$R_2 = \frac{R_{sk}}{2} \quad (3)$$

$$R_3 = \frac{\rho_c}{(\Delta x)^2} \quad (4)$$

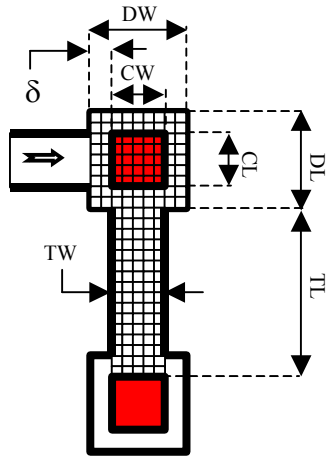

Figure 2 - Modeling of the analyzed region on test structure divided in elementary cubic cells.

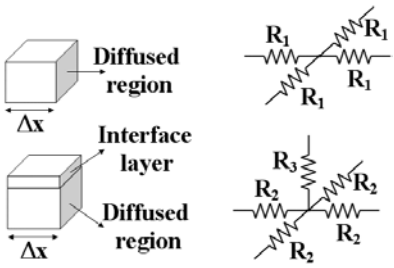

Figure 3 - Analysis of the cubic cells.

All resistor cells were automatically jointed side-by-side, according to the initial specified contact geometry as shown in figure 2. Based on nodal analysis, a linear system of equations was solved using an iterative mode. The voltage drop on the front-end contour (see figure 4) was used to obtain the real contact resistivity as follows:

$$\rho_c = \frac{V_{FRONT}}{I} \times A \quad (5)$$

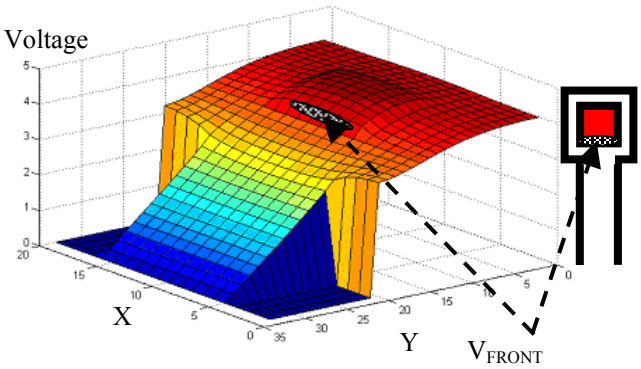

Figure 4- 3D voltage distribution near the contact and the contact front-end region where the front-end voltage is shown.

As already mentioned, the apparent contact resistivity (ρ_c*) is different from the real contact resistivity (ρ_c), because ρ_c*

is affected by the lateral current crowding effect. The program also allows one to obtain the 3D profile of the voltages for each node as shown in figure 4. This program allows a number of nodes as high as 4000 for each analysis.
Furthermore, for the sake of simplicity, it was assumed that the metal layer over the contact region is equipotential. Figure 5 shows the complete flux diagram that was used to obtain the real contact resistivity. In addition, ρ_c* from equation 1 was used as a first estimative of the contact resistivity for an interactive determination of its real value ρ_c (see the flux diagram in figure 5).

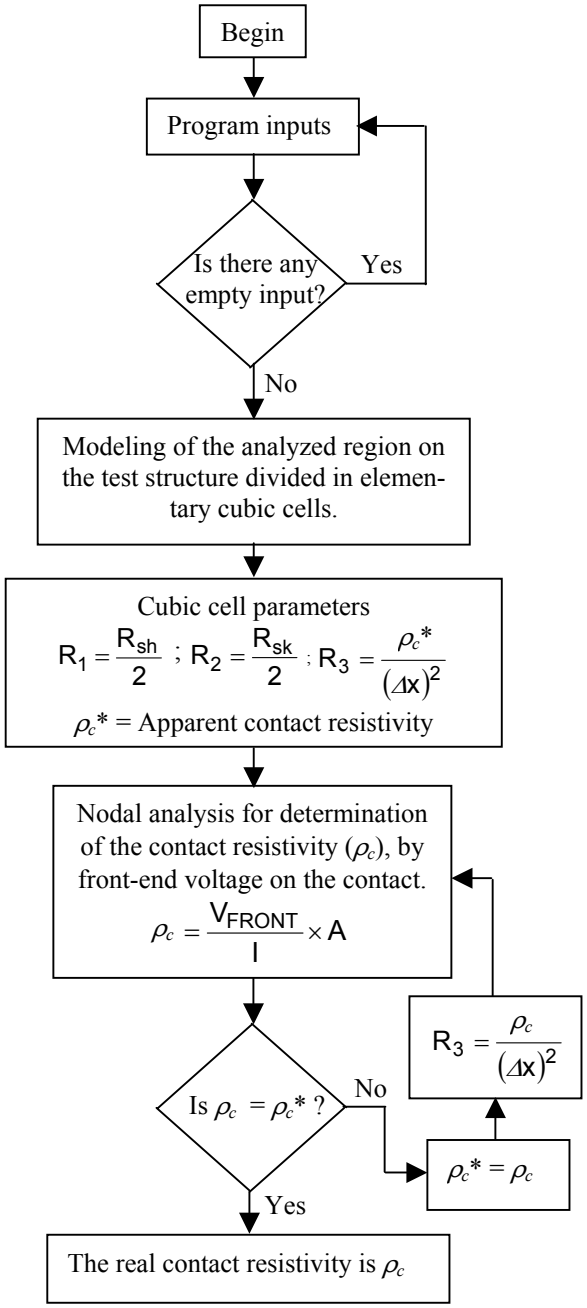

Figure 5 - Flux diagram to determine ρ_c.

3. EXPERIMENTAL PROCEDURE

In this work, p-type silicon (100) wafers, with resistivity of 10Ωcm, were used to produce N$^+$P junctions, 0.6 μm in depth. The samples were implanted with phosphorus at 60keV and doses of $7x10^{15}cm^{-2}$. After the ion implantation, the wafers were annealed at 900°C during 30 minutes in an inert ambient of ultrapure nitrogen. A conventional passivation scheme was used to produce the Kelvin structure (0.8 μm oxide) in order to prevent lateral inversion layer formation. The contacts were produced as cross-bridge Kelvin resistors (see figure 1) using Al over the junction (Al/Si(N$^+$P)) (Wafers-1, 2 and 3) or previous silicidation of the contact followed by Al metallization (Al/TiSi$_2$/Si(N$^+$P)) (Wafers-4 and 5) where TiSi$_2$ was formed in three steps: annealing at 600°C, removal of the non-reacted Ti and rapid thermal annealing (RTA) at 800°C. After the contact-structures production, we have performed the sintering step of the contacts at 420°C (Wafer-1), 435°C (Wafer-2), 450°C (Wafer-3), 420°C (Wafer-4) and 435°C (Wafer-5) during 30 minutes in forming gas atmosphere (N_2+10%H_2). The cross-bridge Kelvin resistors were produced with a contact area of $10x10\mu m^2$ and implanted width around the contact δ=3μm. Therefore, the total implanted area was 16μm x 16μm. Also, the chosen track width was 10μm (TW) and the track length, 50μm (TL) (see figure 2). For the Al/TiSi$_2$/Si(N$^+$P) contacts, the measured sheet resistance of the diffused layer underneath the contact region resulted in Rsk = 3.4 Ω/□ and outside in Rsh = 26.1 Ω/□. For the Al/Si(N$^+$P) contacts, the measured sheet resistance of the diffused layer underneath and outside the contact region resulted Rsk = Rsh = 32 Ω/□.
After fabricating the contacts, measurements were performed with the aid of the cross-bridge Kelvin resistors to determine the contact resistivity. The applied current during the tests was 1mA. We inserted all data in the program, and the used distance among nodes was typically 0.5μm.

4. RESULTS

Table 1 resumes the results for all sintering conditions. The first column presents the structure of contact and each sintering condition. The second column presents the reverse current (J_R) measured at –5V and, the third column presents the apparent contact resistivity (ρ_c*), which was obtained using of the equation 1. The fourth column presents the real contact resistivity (ρ_c) obtained with the aid of the computer program, and, the fifth column presents the relative error between ρ_c* and ρ_c (%). The values of ρ_c* and ρ_c are the arithmetic average of the measurements.
Wafer-1 presented the best result, that is, the lowest values of leakage current density and real contact resistivity. On the other hand, Wafer-2 and Wafer-3 ((Al/Si(N$^+$P)) in spite of presenting low values of contact resistivity, also exhibited prohibitive high values of reverse leakage current after thermal sintering at 435°C or 450°C. The contact resistivity for the Wafer-4 (Al/TiSi$_2$/Si(N$^+$P)) sample resulted high, because of the low sintering temperature of 420°C and the presence of TiSi$_2$ between Al and Si. In this case, it was no-

ticeably that relative error between ρ_c* and ρ_c was as high as 55.2%. On the other hand, Al/$TiSi_2$/Si(N^+P) contacts obtained by sintering at 435°C during 30min (Wafer-5) showed contact resistivity as low as that observed in literature [14, 15] for different contact structures and a relative error of 13.2%.

The time spent by the computer program to solve several interactions until the convergence of the real contact resistivity is about 0.5 second for 100 nodes and 9 minutes for 3024 nodes taking a personal computer AMD Athlon XP 1.16GHz 224MB-RAM as reference.

Table 1 - Reverse current density, apparent and real contact resistivities and relative error.

Contacts	J_R (nA/cm^2)	ρ_c* (μΩcm^2)	ρ_c (μΩcm^2)	%
Wafer-1: 420°C Al/Si(N^+P)	3.0	3.6 ± 1.3	3.3 ± 1.2	8.3
Wafer-2: 435°C Al/Si(N^+P)	1.6 x10^4	5.6 ± 1.9	5.0 ± 1.6	10.7
Wafer-3: 450°C Al/Si(N^+P)	> 10^5	6.2 ± 2.5	5.6 ± 2.1	9.7
Wafer-4: 420°C Al/$TiSi_2$/Si(N^+P)	2.5	147 ± 134	65.8 ± 36.3	55.2
Wafer-5: 435°C Al/$TiSi_2$/Si(N^+P)	2.8	8.3 ± 5.7	7.2 ± 4.5	13.2

Amongst all the program input parameters, only the distance among nodes (Δx) was arbitrarily chosen. However, its value does not alter significantly the final result of the real contact resistivity as shown in figure 6. In this figure, the distance among nodes has ranged from 0.35μm to 7μm, which meant number of nodes between 6120 and 18, respectively. As a result, the real contact resistivity has varied only 4%, that is, a hundred nodes mean a relative error lower than 1%.

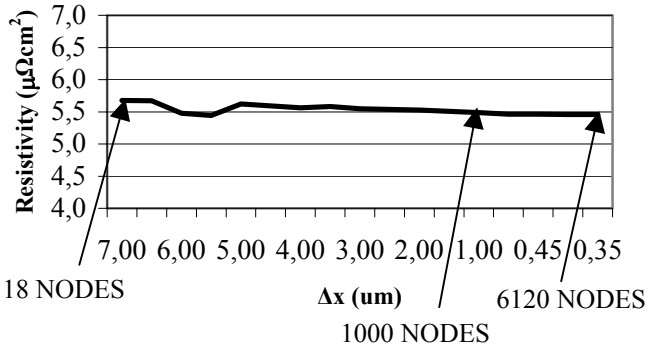

Figure 6 - Real contact resistivity as a function of Δx and amount of nodes.

5. CONCLUSION

For sintering at 420 °C, it was noteworthy to observe high contact resistivity for the Al/$TiSi_2$/Si(N^+P) structure. However, after sintering at 435 °C, the Al/$TiSi_2$/Si(N^+P) structure presented a low contact resistivity of 7.2 μΩcm^2. On the other hand the Al/Si(N^+P) structure, in spite of presenting the lowest value of contact resistivity, also showed prohibitive high values of reverse leakage current after sintering at 435°C and 450°C.

Based on exhaustive simulations using the implemented program, for each sintering, we have observed a decrease, up to 55%, of the real contact resistivity compared to the apparent one due to the lateral current crowding effect. Moreover, we noticed that the result of the real contact resistivity is not strongly affected by the amount of nodes during the simulation.

6. REFERENCES

1. SCORZONI, A., *Materials Science Forum* 881 (2004) 457.
2. SCORZONI, A.; FINETTI, M., *IEEE Transactions on Electron Devices* 35 (1988) 386.
3. SCORZONI, A., *IEEE Transactions on Electron Devices* 34 (1987) 525.
4. WOLF, S., *Silicon processing for the VLSI era. V.2*. Process Integration. Lattice Pres, Sunset Beach (1990).
5. FINETTI, M.; SCORZONI, A.; SONCINI, G., *IEEE Electron Device Letters* EDL-5 (1984) 524.
6. SANTANDER, J.; LOZANO, M., *IEEE Transactions on Electron Devices* 47 (2000) 1431.
7. ONO, M.; NISHIYAMA, A.; TORIUMI, A., *Solid-States Electronics* 46 (2002) 1331.
8. FURLAN, R. *Estudo da formação e das características de contatos Al/TiW/$TiSi_2$ sobre junções rasas com aplicação da técnica AES.* Tese de Doutorado (1990). Escola Politécnica, Universidade de São Paulo (SP).
9. SANTANDER, J.; LOZANO, M., *IEEE Transactions on Electron Devices* 40 (1993) 944.
10. OHRING, M., *Materials Science of Thin Films-Deposition and Structure*. Second Edition, Academic Press, San Diego, 2002.
11. MARTINO, J.; PAVANELLO, M.A.; VERDONCK, P. B., *Caracterização elétrica de tecnologia e dispositivos MOS*, Thomson, São Paulo, 2003.
12. SCORZONI, A.; FINETTI, M., *Advanced metallization for VLSI/ULSI applications - III Brazilian Microelectronic School*, UNICAMP, São Paulo, 1994, p. 81.
13. BRESSE, J.F.; BLAYAC, S., *Solid State Electronics* 45 (2001) 1071.
14. TING, C.Y., *IEDM Tech. Dig.*84 (1984) 110.
15. MURARKA, S.P., *Silicides for VLSI applications*. New York: Academic, 1983.