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COMPARISON BETWEEN CONDUCTIVE AND NON-CONDUCTIVE TIPS FOR LOCAL ANODIC OXIDATION

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ABSTRACT

Local anodic oxidation of silicon using Atomic Force Microscopy (AFM) was investigated by applying a negative voltage between conductive (Au coated silicon or silicon nitride) or non-conductive (silicon nitride) tips and Si surfaces. All samples were cleaned with an ammonium-based solution known in literature as standard cleaning 1 (SC1) or a dip in a diluted hydrofluoric acid solution followed by SC1 cleaning step. Localized squares patterns of oxide, 0.25 μm² in area, were formed by growing parallel lines with constant interlinear spacing and length after scanning several times in the same area. From AFM analysis with non-biased tip, it was obtained 3D and section profiles. Simulations were performed in order to model voltage and electric field distributions of the system tip-air-silicon or tip-air-oxide-silicon. In addition, it was simulated the effect of tip termination, circular or sharpen, considering electric field and voltage distributions. Finally, anodic oxidation using non-conductive silicon nitride tip or conductive tips were performed and compared.

1. INTRODUCTION

Atomic Force Microscopy (AFM) has been used in the field of nano-lithography. In particular, this technique has been successfully used for patterning various nano-devices including quantum-point contact [1,2], single-electron and field effect transistors [3-6], masks for selective etching [4,7], and contact pads [8]. The research in the field of nano-lithography presents several advantages including simplicity to reach the nanometer scale and to visualize the generated patterns with the same equipment [9].

One AFM technique used to produce high quality oxide patterns as mask onto silicon surfaces is the Local Anodic Oxidation (LAO) [10-15]. The local oxidation of silicon is based on an anodization mechanism assisted by a high electric field ($\geq 1 \times 10^7$ V/cm) between conductive tips and silicon surfaces [16]. Gordon et al. has shown a model based on a diffusion-limited anodization due to a high electric field (2×10^7 V/cm) [16]. During the anodization process, the oxide thickness increases and the electric field through the oxide decreases. The process is self-terminated when the electric field becomes sufficiently low so that the ionic diffusion of species ceases [16,20]. The thickness of the oxide layer generated using this technique ranges typically from 1 and 10 nm.

It is well known that the oxide thickness is a linear function of the anodic voltage and an exponential function of the oxidation time [9,10,12-15,17-19]. Many factors, such as scan speed and contact force may affect the thickness during local anodic oxidation, however, it has been widely accepted that the mentioned strong local electric field between silicon and tip is the detrimental first-order parameter [15]. Also, large area oxidation has been obtained by growing parallel lines with small interlinear spacing in order to fabricate nano-devices with different geometries [20].

Another important parameter is the pre-oxidation cleaning step. The most studies used hydrogen-terminated Si surfaces after dipping in diluted HF [14-16]. On other hand, some authors have also reported anodization process (LAO) on oxidized Si surfaces [9,12].

In this work, it was investigated LAO using different types of tips onto silicon surfaces. Specifically, a comparison between conductive and non-conductive tips for anodic oxidation was performed.

2. EXPERIMENTAL PROCEDURE

For local anodic oxidation, it was used p-type (111) silicon samples with resistivity in the range of 0.008 to 0.02 Ωcm or n-type (100) silicon surfaces with resistivity around 0.1 Ωcm. All samples were cleaned using a SC1 procedure (boiling in 4 NH_4OH (30%): 1H_2O_2 (38%): 1H_2O (DI)) (21,22), some of them were previously dipped in a diluted HF solution (20 H_2O(DI): 1 HF (49%)) in order to remove the former native oxide before SC1. The AFM equipment used in all experiments was the Nanoscope E from Digital/Veeco with a 15-nm or 30-nm Au coated silicon tips or 15-nm Au coated silicon nitride tips with radius in the range of 10 to 20 nm. The negative voltages applied between the tip and the samples (V_{tip}) were: -5.0 V and -10.0 V. For each voltage, square patterns of oxide, 500 x 500 nm² in area, were formed by growing parallel lines with constant interlinear spacing (< 2nm) repeated one or two times in the same area (1 or 2 scans). Figure 1 shows the experimental setup for the local anodic oxidations including typical dimensions of the tip and cantilever. The previous cleaned silicon sam-

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ples were fixed onto a metallic sample holder using carbon glue (figure 1).

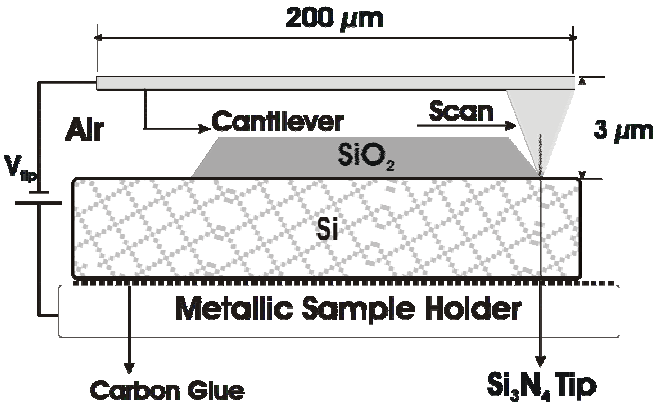

Fig. 1 – Experimental setup for local anodic oxidation.

At first, 500nm-square scans were extracted with the aid of contact-mode AFM and without any applied voltage. Following, in the same region, a given negative voltage was applied using an HP E3631A for the anodic local oxidations. In order to investigate if silicon oxidation occurred, two AFM analysis were obtained without any applied voltage at higher scan sizes: one at 5μm and another at 2μm so that the previous oxidized region were inside of the measuring scan. From the measurements, 3D and section profiles were taken and the step height was extracted at the border of the oxidized patterns. The oxidations were performed after the cleaning steps using smaller voltages compared to the ones that were used to perform local anodic oxidation with non-conductive tips [23].

In order to perform the simulations, finite-element method was used with the aid of the QuickField 5.3 finite element analysis system [24]. Simulations were performed by solving the Poisson discrete equation taking into account the system formed by the tip (conductive or non-conductive), the air, the Si sample and, in some cases, a thin native oxide layer between the tip and the Si surface.

Based on the simulations using a negative voltage at the cantilever top (-20 V), the voltage drop across the tip and electric field at the tip apex were obtained for different tip terminations, circular or sharpen.

3. RESULTS AND DISCUSSION

Au coated Si tips showed very good performance for anodic oxidation and they were less susceptible to Au delamination compared to Au coated silicon nitride tips. For thickness smaller than 15nm, delamination never occurred whereas, for 30-nm Au coatings, delamination occurred and the silicon-nitride tips became useless even to measure topography or to perform nano-oxidations. On the other hand, silicon tips that were recovered with 30 nm of Au presented no delamination during local oxidations.

Anodic oxides were obtained on p-type (111) and n-type (100) silicon samples, cleaned using a dip in a diluted HF solution followed or not by SC1. Figure 2 shows oxides grown on p-type (111) silicon samples after two scans and with anodic voltage of -5V using 30-nm Au coated silicon tips (figure 2.a) and 15-nm Au coated silicon nitride tips (figure 2.b). Both were cleaned in diluted HF solution followed by a SC1 step. As a result, it was observed well-defined oxide patterns for both types of tip.

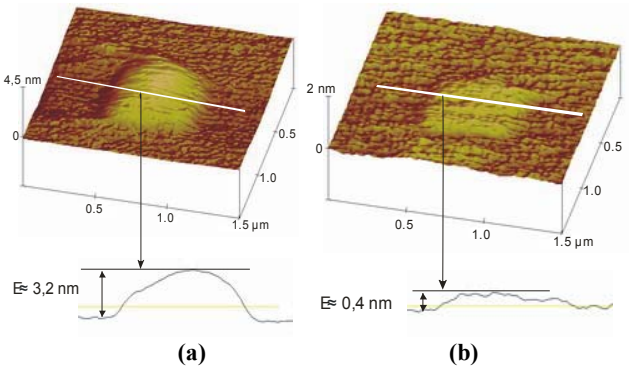

Fig. 2 – Localized anodic oxides grown on p-type Si (111) samples after 2 scans and with anodic voltage of - 5V using: (a) 30-nm Au coated silicon tip and (b) 15-nm Au coated silicon nitride tip. The samples were cleaned in diluted HF solution followed by a SC1 cleaning step.

As shown in figure 2, it can be observed that the type of tip influences the oxide thickness. For 30-nm Au coated silicon tips, we obtained anodic oxides with an average thickness of (3.23 ± 0.13) nm while, for 15-nm Au coated silicon nitride tips, the average thickness obtained was (0.41 ± 0.07 nm), this is to say, it is substantially smaller. Possibly, the quality of the Au coating was better over silicon tips and it can be inducing higher electric fields at the tip apex.

In figure 3, it is shown an anodic oxide obtained over a p-type silicon sample after 2 scans with an anodic potential of -5V using 30-nm Au coated silicon tips. In this case, the cleaning consisted of dip in diluted HF solution (1 HF(49%):20 H_2O during 60 s. Comparing figure 2a with figure 3, under the same anodic oxidation condition using the same type of tip but, with an additional SC1 cleaning step, it was observed that the anodic oxides formed after the additional SC1 step presented a higher thickness compared to anodic oxides formed after dipping in diluted HF solution [(0.81 ± 0.04) nm]. This observation indicates that the final SC1 cleaning step may induce superficial changes consistent with a higher oxidation rates. As the surface became hydrophilic after the SC1 cleaning step, the presence of water molecules may be favoring the oxidation process.

The n-type Si samples, oxidized under anodic potentials in the range of -5 to -10V (2 scans), presented well-defined oxide patterns with good reproducibility. Figure 4 shows an oxide pattern obtained on an n-type Si (100) sample after 2 scans with an anodic voltage of -5V. The final oxide thickness [(3.39 ± 0.13) nm] over n-type Si resulted similar to

that thickness obtained over p-type Si samples, indicating that the type of substrate does not affect the oxidation thickness for samples previously cleaned with the same SC1 step.

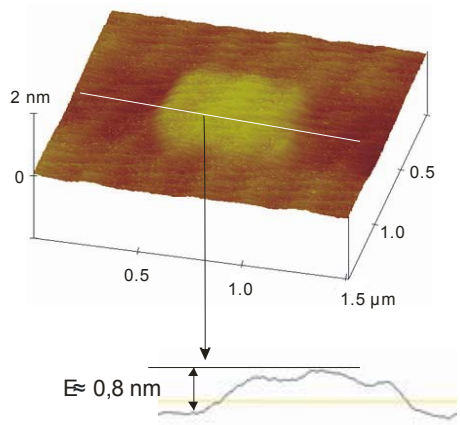

Fig. 3 – Localized anodic oxides performed over p-type Si (111) samples after two scans under an anodic potential of - 5V using 30-nm Au coated silicon tips. Si was previously cleaned with a dip in a diluted HF solution during 60 s.

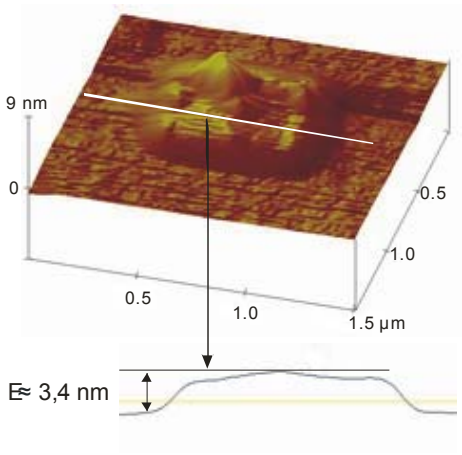

Fig. 4 - Localized anodic oxide obtained on n-type Si (100) samples after two scans, at an anodic voltage of -5V using 30-nm Au coated silicon tips. The sample was previously cleaned in diluted HF solution followed by a SC1 cleaning step.

It is important to point out that, after applying voltage on the coated tip, it did not happen any vertical dislocation of the cantilever as in the case for silicon nitride tip [23], possibly because the charging of the conductive tip is lower compared to the charging of non-conductive tip since there is a path to drain the charges in the first case. Besides, for non-conductive tips, a similar phenomenon happened as for conductive tips, this is to say, the SC1 final cleaning step provided favorable condition to LAO process resulting in oxides with higher thickness compared to the samples cleaned with dip in diluted HF solution followed by SC1 [23]. The final thickness obtained over n-type Si (100) resulted similar to that thickness obtained over p-type Si (111) because the last cleaning step must be being the main first order parameter independent of the type of the substrate.

Table 1 shows the results of simulation for sharpen and circular tip termination, with and without a 1-nm thin oxide layer between the tip and the Si sample.

Table 1 – Electric field and voltage at the tip apex for different tip materials and terminations.

Tip's kind and simulation condition	Voltage at the tip apex (V)	Electric field at the tip apex (10^5 V/cm)
Sharpen non-conductive tip termination	-8.21	7.72
Circular non-conductive tip termination	-8.37	1.28
Sharpen conductive tip termination [12]	-7.50	300.00
Circular conductive tip termination [12]	-7.50	155.00

It is noteworthy that the voltage at the cantilever top for non-conductive tips was fixed at -20 V, resulting about -8 V at the tip apex. For conductive tips, the voltage at the cantilever top was fixed at -7.5 V and there was not a voltage drop across the tip, resulting -7.5 V at the tip apex (the same voltage applied at the cantilever top). On the other hand, the electric field at apex of the non-conductive tip resulted almost two orders lower than the electric field for conductive tips.

It is important to point out that, even for non-conductive tips or conductive tips there is a substantial electric field diminishing when the tip termination is changed from sharpen termination to circular one. In this last case, the electric field becomes distributed around the tip radius, while, for sharpen tips, the electric field is focused on the apex as shown in table 2.

Table 2 – Simulated electric field and voltage at the tip apex considering a between tip and Si for different non-conductive tip terminations.

Position	Tip termination	Voltage at the tip apex (V)	Electric field at the tip Apex (10^5 V/cm)
At the tip apex	Sharpen	-10.75	18.04
	Circular	-10.92	18.66
At the SiO_2/Si interface	Sharpen	-10.58	5.31
	Circular	-10.65	5.86

Comparing table 1 with table 2, it is noteworthy that the native oxide layer (1nm) decreases the electric field at least one order of magnitude at the SiO_2/Si interface for the non-conductive tip. In addition, the presence of the native oxide also decreases the electric field for conductive tips with sharpen and circular termination (not shown in the tables).

4. CONCLUSION

Local anodic oxidation (LAO) of silicon using Atomic Force Microscopy (AFM) was investigated by applying an anodic voltage between an Au-coated silicon nitride tip or silicon tip and p^+ or n^+ doped Si (111) surfaces. All samples were cleaned with an ammonium-based solution known in literature as standard cleaning 1 (SC1) or a dip in a diluted hydrofluoric acid solution followed by SC1. The negative voltages applied were -5 and -10 V. It was investigated LAO focusing on the comparison of conductive with non-conductive tips. On the other hand, this is the first work that compares the use of non-conductive and conductive tips for local anodic oxidation taking into account the cleaning process used.

Localized square patterns of oxide were grown after 2 scans and the step height was measured with the aid of contact-mode AFM without any applied voltage between the tip and the sample. The main results were: (a) the anodic voltage for LAO using conductive tips were smaller than the voltage applied for non-conductive tips; (b) the thickness did not vary significantly with the type of the substrate (N or P) and (c) the silicon tips are better to be coated than silicon nitride tips because Au presented better adherence on Si tips. On the other hand, the oxide thickness was higher when the last step of the pre-oxidation cleaning was SC1 because surface becomes hydrophilic and the presence of water molecules may be favoring the oxidation even for lower electric fields which are at least one order of magnitude lower for non-conductive tips.

The simulations showed electric fields almost two orders lower for non-conductive tips compared to that for conductive ones. In addition, there was a voltage drop across the non-conductive tips which meant higher anodic voltages for this case.. Finally, for both types of tip,, the circular termination presented lower electric field at the tip apex compared to the sharpen termination. On the other hand, a native oxide between the tip and the sample decreased the electric field at the SiO_2/Si interface for non-conductive and conductive tips.

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