HIGH PERFORMANCE THIN-FILM TRANSISTORS FOR LIQUID CRYSTAL DISPLAYS

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ABSTRACT:

Various possible applications have been reviewed of thin-film transistor-matrix driven liquid-crystal displays. Novel process technologies have been discussed aiming at high performance thin-film transistors on glass substrate. It has been concluded that the most promising deposition technology is of a low-temperature chemical-vapor-deposition method using higher silanes and nitrogen compounds. Good amorphous-silicon and silicon-nitride films can be deposited at temperatures of as low as 350°C. For on-chip peripheral circuits, an excimer-laser crystallization method seems the most promising, since high temperature can be applied to the semiconducting film while keeping the substrate at the room temperature. The mobility of as high as 380cm^2/Vs has been achieved by this method.

1. INTRODUCTION

It is only recently that everybody understood an importance of flat-panel displays. And now, it became well known that the thin-film transistor (TFT) matrix-drive is a decisive factor for attaining the high-quality flat-panel displays.

Applications of these displays are divided into two fields, i.e., a direct view and an indirect view. For indirect view applications, panel size is in a range from as small as 0.7" to about 3". Major products are of a view finder in cameras and of a projection display. For direct view application, the display is about 5" in diagonal size for toys and potable TVs, and more than 10" for Engineering Work Stations. 10.4" color displays are now used in book-type PCs. The maximum size of the display reported to date is 15" having more than 3 million dots. A very large market is expected also in multi-media including virtual reality systems.

Rapid development of display technology, however, made clear the fact that there are fatal drawbacks of the present device/process technologies. Especially, plasma-CVD method, the most representative deposition method, has serious problems arising from its inherent properties. Thus the novel technology should be developed where the semiconductor film and the insulator film can be deposited under low temperature conditions without plasma.

Question has been arisen on driving capability of amorphous-silicon (a-Si) TFTs, i.e., the representative TFT, for future ultra-high quality displays aiming at, for example, high-definition TV receivers. This is because the field-effect mobility of the a-Si TFT is still less than 1cm^2/Vs. For the denser, larger and high-speed displays, the a-Si TFT seems not acceptable. Thus various efforts are paid to high mobility poly-Si TFTs.

This paper reviews novel process for the next generation TFT matrix.

2. CVD TECHNOLOGY for a-Si TFT

2.1 Problems of plasma-CVD Method

Major technological driving force for the rapid growth of the a-Si TFT was not the chemical-vapor deposition (CVD) method [1], the dominant thin-film deposition method in VLSI process, but the plasma-enhanced CVD (plasma-CVD) method [2], which had been originally developed for a-Si solar cells. This is because the deposition temperature should be much lower in the TFT process based on a glass substrate than in the VLSI process. This threw away whole advantages of the thermal-CVD method over the plasma-CVD method.

The present plasma-CVD method, however, has serious problems for future flat-panel displays, such as (1) dense pinholes especially in the deposited insulator film due to dust generated in the plasma-CVD chamber, (2) low throughput, (3) low film quality, and (4) lack of reproducibility in the film quality, all of which come from inherent properties of plasma as follows.

Frequent collision of high energy particles in gas phase is the driving force of sustaining plasma. Since plasma-polymerization is triggered by collision of silane-hydride radicals with neutral silane molecules, plasma generates inevitably many particles. And dense flax of radicals formed uniformly in the plasma, hits the chamber-wall and RF electrodes, resulting in the thick deposited film on them. Thermal peeling-off of the deposited film generates dense flakes.

It should be noted also that frequent cleaning of the deposition chamber for reducing density of dust elongates the total down-time and that the cleaning also makes difficult to bake-out the chamber sufficiently, resulting in inferior film properties and reproducibility. There is so-called plasma-damage caused by the fact that high energy electrons and ions attack the deposited film surface, resulting in the deterioration

of the film properties. The fact that there are too many plasma parameters results in the lack of reproducibility. Large potential gradient in the plasma makes difficult for the film to grow simultaneously over many substrate surfaces stacked in the chamber.

2.2 Features of thermal CVD method

Typical CVD temperatures were more than 550°C for the a-Si film and 800°C for the silicon nitride (SiN_x) film, respectively. Since these extremely high deposition temperatures are caused by large chemical binding energies of Si-H bonds in mono-silane (SiH_4) and of N-H bonds in ammonia (NH_3), the temperature can be reduced drastically by introducing higher silanes, such as di-silane (Si_2H_6) or tri-silane (Si_3H_8) having weak Si-Si bonds, together with higher nitrogen compounds such as hydrazine (N_2H_4) or hydrogen azide (HN_3) [3] having weak N-N bonds. Since the CVD method has no inherent shortcomings caused by plasma [4,5], the film can be deposited with high throughput and with good electronic properties. There are only four deposition parameters, i.e., temperature, total pressure, partial pressure and flow rate, and thus good reproducibility can be easily obtained. Batch processing has been already demonstrated [6]. The CVD method has additional features as follows.

Due to rather high CVD temperatures, silane-hydrides can migrate on the surface for a long distance, and thus they have many chance for finding the site with the lowest potential energy. The film has good short-range order, and low hydrogen content, i.e., high packing density, due to high deposition temperature will enhance this preferable property. Good short-range order of the CVD film results in the superior electronic properties, such as high carrier mobility and low tail state density.

There are dense dangling bonds in the as-deposited a-Si film. However, these bonds can be terminated by post-hydrogenation [7]. Processing with rather high temperature is acceptable if it is lower than the CVD temperature, since post-hydrogenation done at the final process step terminates dangling bonds formed by the high temperature pre-steps.

2.3 Experimental

Apparatuses we have used are schematically shown in Fig.1 for the CVD [8] and Fig.2 for the post-hydrogenation

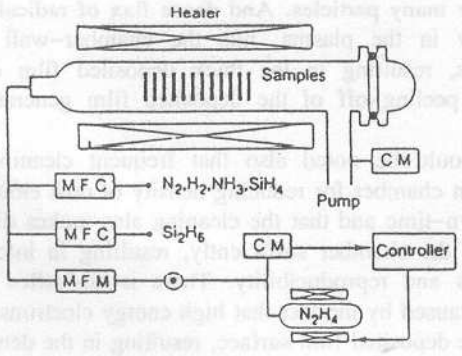


Fig.1 Hot-Wall CVD System

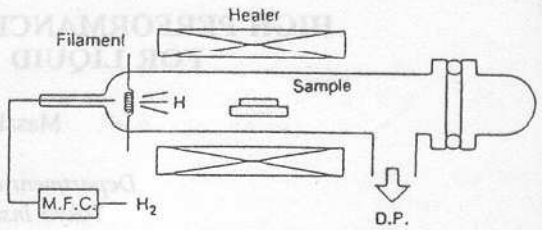


Fig.2 Hot-Wall Hot-Filament Post-Hydrogenation System

[7], respectively. Both apparatuses were of hot-wall type and operated at pressures of as low as 1Torr. Thus they can be enlarged for practical substrate size without serious modifications, and will be used for stacked substrates.

At the deposition rate of 1nm/min, the a-Si CVD temperature was as high as 650°C for SiH_4, but reduced to 500°C for Si_2H_6 and to 450°C for Si_3H_8, respectively. For the SiN deposition, a gas mixture of Si_2H_6 and N_2H_4 could deposit the film at 530°C and a mixture of Si_3H_8 and HN_3 at 450°C. Application of tetra-silane could reduce the temperatures below 400°C.

The bottom gate CVD a-Si TFT with the CVD SiN gate dielectric has been fabricated at 500°C using a mixture of Si_2H_6 and N_2H_4. Semi-logarithmic TFT characteristics are shown in Fig.3. Large current under positive gate voltage, V_g, is caused by electron conduction and large current under negative V_g by hole conduction since there is no blocking contact for both carriers at the source and drain. Thus the characteristic curve had a V-shaped form. Electron mobility was as high as 1.5cm^2/Vs and hole mobility about 0.1cm^2/Vs, respectively.

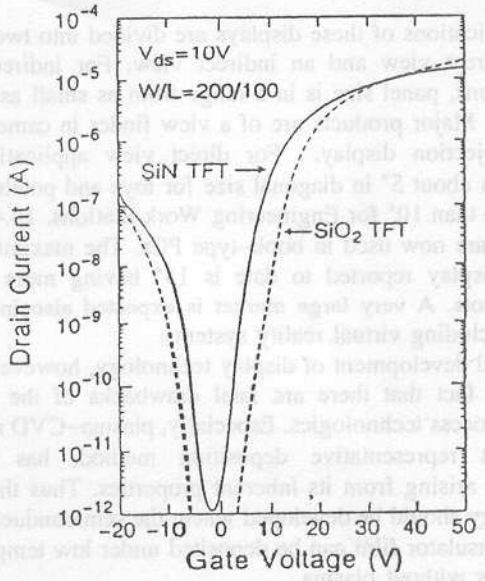


Fig.3 Characteristics of bottom Gate CVD a-Si TFTs with SiO_2 and CVD SiN_x gate

The CVD a-Si TFT has been also fabricated using thermal oxide as the gate dielectric at various a-Si deposition temperatures and using various source gases. Results are shown in Fig.4 as a function of the deposition temperature. Electron mobility of the as-deposited TFT was about 0.6cm^2/Vs at 350°C and decreased gradually with increasing the temperature due to decreased hydrogen content. But the mobility after post-hydrogenation went up to more than 1cm^2/Vs and increased with the deposition temperature to more than 2cm^2/Vs.

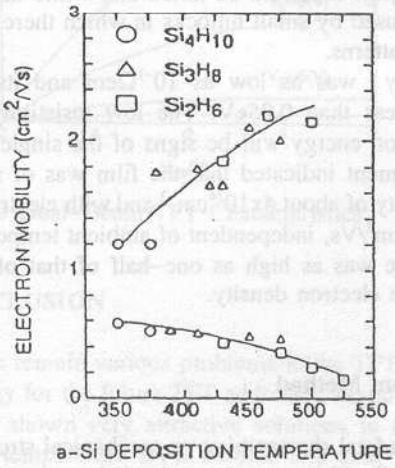
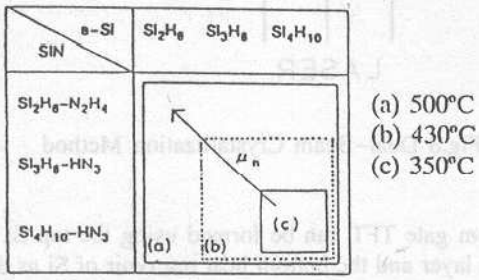


Fig.4 Field-Effect Mobility as a Function of CVD Temperature

Effects of deposition parameters are investigated on the deposition characteristics and the TFT characteristics. The high temperature improves the TFT characteristics only gradually, but increases the deposition rate exponentially. The increase of partial gas pressure increases the deposition rate, but does not change the TFT characteristics. Total pressure has no large influences. Thus we can conclude that batch process can be easily attained by tuning the temperature profile along the gas flow.

Figure 5 summarizes the best gas combination as a function of the deposition temperature. When 500°C is acceptable, the Si_2H_6 and N_2H_4 mixture is the best and the mobility will be more than 2cm^2/Vs. When the highest temperature is 430°C, Si_3H_8 and HN_3 should be used and the mobility will be reduced to about 1.5cm^2/Vs. When the temperature should be as low as 350°C, Si_4H_{10} should be used instead of Si_3H_8 and the mobility will be as low as 1cm^2/Vs.



(a) 500°C
(b) 430°C
(c) 350°C

Fig.5 Best Combination of Source Gases

3. Poly-Si TFT TECHNOLOGY

3.1 Features of Excimer Laser Crystallization Method

There are three methods to form poly-Si on glass substrate, i.e., the deposition method, solid phase growth method and laser crystallization method. High quality poly-Si film can be obtained only by the laser crystallization method. This is because only this method can heat up the film to the melting point of Si without introducing serious thermal damage to the glass substrate.

Among various laser crystallization methods, the excimer-laser method seems the most promising. This is because only this method has a sufficiently high throughput. Another potential advantage of this method is that there are several lasers having different properties. For example, the XrF laser light has a photon energy of as small as 3.5eV and thus can pass through various insulators including glass substrate, but has the sufficiently high absorption coefficient to Si. The ArF laser light, on the other hand, has the photon energy (6.4eV) much higher than the SiN bandgap (about 5eV). Thus the ArF laser can heat up the SiN film to very high temperature, resulting in the improved SiN film properties. There is still a serious barrier in this method that the typical mobility value is as low as 100cm^2/Vs [6], i.e., about 1/10th of the electron mobility in bulk Si. This is because motion of electrons is seriously disturbed by the potential barrier formed at the grain boundary in the poly-Si film, and because the typical grain size is much less than 0.1μm. Hydrogenation of the grain boundary reduces density of deep traps, and thus suppresses unwanted effects caused by the grain boundary [7]. Its usefulness, however, is limited. In order to increase the carrier mobility drastically, the grain size should be increased.

Among various factors which cause the grain size to a small value, the generation rate of nucleus and growth rate of nucleus will be the dominant factors. Since both of them are related with the transient temperature profile, it can be said that the solidification rate of the molten Si film is the predominant parameter which determines the grain size of the excimer-laser crystallized Si film. In case of the conventional method, the 100nm-thick molten Si film is completely solidified within 100ns. The solidification rate is extremely high (more than 1m/s).

3.2 Proposed Bridge Structure

Cross section of the proposed bridge structure is shown in Fig.6 [10]. The thin Si film is formed on the thin SiO_2 membrane, which has been constructed by removal of (111)Si substrate using preferential wet etching after thermal oxidation. Just after the laser irradiation, latent heat stored in the molten Si film is diffused into the substrate made of SiO_2 membrane, and thus the molten Si film starts to be solidified rapidly from the Si/SiO_2 interface, as in case of the conventional method. There is also no large temperature difference along the interface. This vertical solidification is, however, stopped in our structure within a short time due to the fact that the whole membrane is heated up to the melting temperature of Si. Then

the resultant latent heat stored in the molten Si film should be lost by thermal conduction along the interface. Since the membrane is very wide, the heat removal rate is drastically reduced. Furthermore, there appears a temperature gradient along the interface, i.e., the temperature is the highest at the center of membrane and the lowest at the edge. Thus the lateral solidification appears, i.e., the molten Si film starts to be solidified from the edge and remains in a liquid state for a long time at the center. Not only the low solidification rate but also the lateral growth of grains will be very effective for enlarging the grain size.

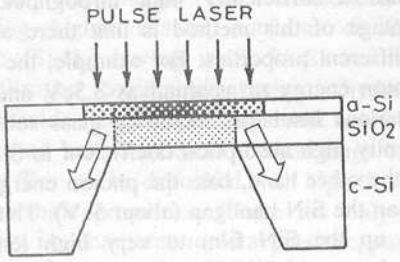
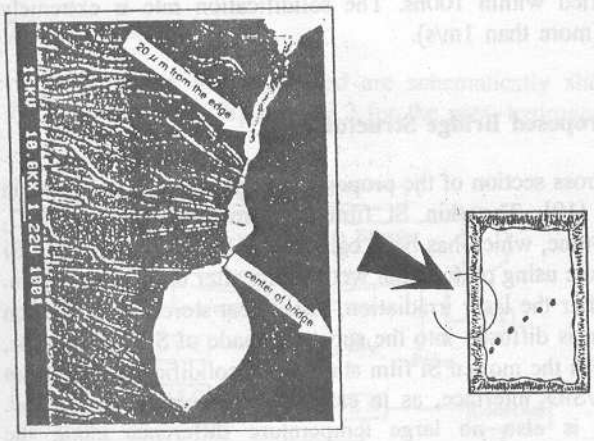


Fig.6 Schematics of Bridge Method

3.3 Experimental

The 40nm-thick a-Si film was deposited on the Si substrate with the SiO_2 membrane at 460°C by low-pressure CVD method using disilane. The Si film was then crystallized by irradiating single-shot ArF excimer-laser light pulse in a vacuum chamber.

When E_l was 350mJ/cm^2 the surface on the membrane was specular with several hillocks, but was changed to have clear patterns after secco etching. SEM photograph is shown in Fig.7(a) for the secco etched surface near the edge of the membrane. There were many stripe-like patterns near the edge directing the center of the membrane as schematically shown in Fig.7(b). Typical length and width of the pattern were about20μm and 2μm, respectively. These aligned patterns can be explained to be caused by lateral epitaxy which was triggered by the drastically reduced lateral solidification rate. The stripe pattern, however, disappeared suddenly, and there was a flat surface region having no etched pattern. This region can be considered as a single grain. The grain size was thus more than 50μm. It should be noted that white images in the figure was caused by small hillocks in which there were many fine etched patterns.



(a) (b)

Fig.7 SEM photograph after secco-etching

Resistivity was as low as $10^{-1}\Omega$cm and its activation energy was less than 0.05eV. The low resistivity and very small activation energy will be signs of the single grain. The Hall measurement indicated that the film was of n type with electron density of about 4×10^{16}cm^{-3} and with electron mobility of about 610cm^2/Vs, independent of ambient temperature. The mobility value was as high as one-half of that of crystal-Si with the same electron density.

3.4 Dual Beam Method

There is a fatal shortcoming on mechanical strength in the bridge method. This can be solved by a novel method schematically shown in Fig.8 [11]. A three-layer structure of Si/Insulator/Heat reservoir is formed on the glass substrate. Laser beams are irradiated simultaneously from both sides. Since the bottom heat reservoir prevents rapid heat removal from the top Si layer, the solidification rate of the Si film is reduced as in case of the bridge method. Average grain size obtained to date is 0.8μm.

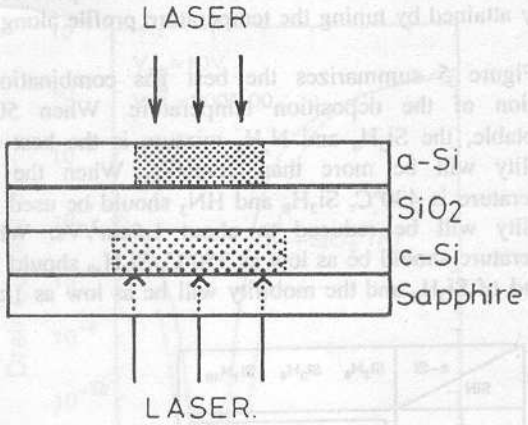


Fig.8 Dual-Beam Crystallization Method

Bottom gate TFT can be formed using the top Si film as the active layer and the bottom heat reservoir of Si as the gate. The TFT characteristics are shown in Fig.9. The mobility was as high as 380cm^2/Vs.

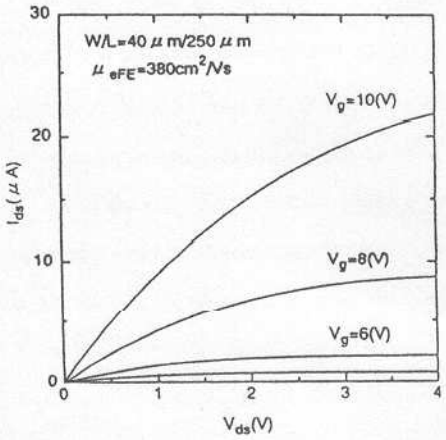


Fig.9 Dual-Beam TFT Characteristics

4. CONCLUSION

There remain various problems in the TFT device/process technology for the future TFT addressed liquid crystal display. We have shown very attractive solutions to these problems, i.e., low-temperature CVD method and dual-beam excimer-laser crystallization method.

ACKNOWLEDGEMENT

The author would like express his thanks to his co-working members. Higher silanes were presented by Showa-Denko.

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