SEMICONDUCTOR PROCESSING: A 1.25 MICRON CMOS PROCESS AND AN AMORPHOUS SILICON THIN FILM TRANSISTOR LARGE AREA LIQUID CRYSTAL DISPLAY.

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We describe two semiconductor processing developments. One of them is a 1.25 micron design rule CMOS process that is fully operational with good yield in a Class 100 clean room. The method of contrast enhanced lithography (CEL) is used for pattern definition. The techniques of planarization and gate sidewall spacers is described. A second semiconductor process that is under development is for producing field effect transistors in a matrix array using amorphous silicon deposited on glass in a plasma enhanced CVD system. There are 160,000 transistors in the present 10cm X 10cm array. Each transistor controls the voltage of an indium tin oxide pixel (transparent and conductihg). A color filter with red, green, and blue elements forms the second parallel plate, with the liquid crystal in between. Transmitted light through the liquid crystal and color filter is controlled by the amorphous silicon FETs.

VLSI, a-silicon, display

I. INTRODUCTION.

This paper will describe two different examples of silicon processing that are being developed at the author's institution (General Electric Research and Development Center). The first of these is known as an A/VLSI process (advanced VLSI) with 1.25 micron design rules in single crystal silicon. Important in the development of this process is the use of contrast enhanced lithography (CEL), the use of oxide sidewall gate spacers, and the use of planarization. The second process under development is a large area video liquid crystal color display with an X-Y addressed matrix where each pixel element is controlled by an individual amorphous silicon field effect transistor. It is an example of the use of amorphous silicon for a large area device on a transparent substrate, where the processing temperatures must be kept lower than the melting point of the substrate glass.

II. The A/VLSI 1.25 MICRON CMOS PROCESS.

We will describe the general process flow, and some of the salient techniques and processes involved. Some of the steps including implants for threshold adjust and punchthrough control are omitted for the sake of brevity. The starting material is N-type single crystal silicon. Epitaxial silicon is used when increased radiation hardness and resistance to latch-up is desired.

The process uses a twin tub technique in which the NMOS and PMOS devices are fabricated in their own tubs and are independently optimized. The LOCOS (Local Oxidation of Silicon) technique is used to form the side walls of the tubs. This process is depicted in Figure 1. A thin oxide layer is grown on the surface, followed by deposition of LPCVD nitride. The oxide serves as a stress relief interface between the silicon and the nitride. The nitride is then patterned and etched in hot phosphoric acid to delineate and protect the NMOS and PMOS regions. The stress relief oxide is then removed except where it is covered by the nitride. The field oxide which separates the NMOS and PMOS regions is then thermally grown, and the rest of the nitride is removed, leaving the characteristic bird's beak oxide at the edge of the wells that is typical of this process.

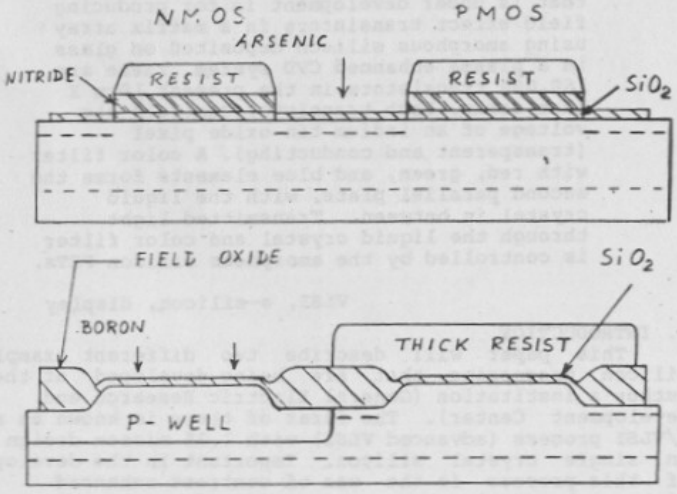

Fig. 1. Two successive cross-sectional views of the the A/VLSI process during fabrication showing LOCOS isolation and Retrograde P-well with bird's beak field oxide.

At this point we mask the N-well and form the P-well by implanting a large dose of boron at a high energy. This is called a retrograde implant because the peak of the boron concentration is well below the surface, giving a retrograde shaped distribution. Following the retrograde implant, very high temperatures are avoided for the rest of the process to prevent significant redistribution of the retrograde implant.

The screen oxide is stripped, and a 250 angstrom gate oxide is thermally grown, using TCA (trichloroethane) as an additive. The chlorine in the oxide tends to tie up free sodium that may be present. The location of the chlorine is shown in Fig. 2, which gives a SIMS profile for chlorine (1). In this figure a 1000 A oxide was grown thermally over a silicon substrate without chlorine. This was followed by growing a 250 A thermal oxide using TCA at a level of 4% equivalent HCl. It is seen that the clorine tends to diffuse from the thin oxide in which it was deposited through the original oxide to the silicon/oxide interface. This is exactly where one would want it to immobilize any free sodium. Apparently the high concentration of fixed positive charges near the Si/SiO2 tends to trap the chlorine.

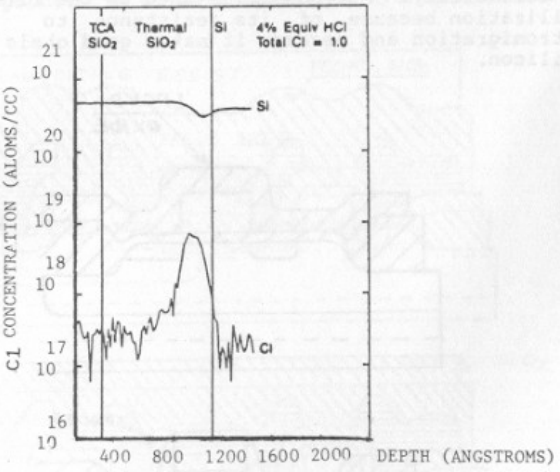

Fig. 2. SIMS data showing concentration of chlorine in 250 A oxide grown in TCA over a 1000A oxide grown without TCA.

Following the gate oxide, a polysilicon layer is deposited using LPCVD to form the gates. The polysilicon is 4000 angstroms thick and is doped with POCl3 to lower the sheet resistance to about 35 ohm/square. Lightly doped drain (LDD) structures are used to reduce the high fields otherwise present in short channel length devices. Light implants of arsenic and phosphorus are given in the N+ regions, the rest of the wafer being masked. The energy

of the implant is as high as possible without the implant penetrating the polysilicon gate. The choice of this lightly doped drain was made on the basis of device modeling and experimental measurements with accelerated hot electron lifetime testing.

Sidewall oxide spacers are used to shift outward from the channel edges the source and drain implants to reduce the lateral doping gradient of the NMOS junctions that are blended with the lighly doped drain implants. The sidewall spacers are formed by depositing a CVD (chemical vapor deposition) oxide that is conformal to the surface (Fig. 3). This is then etched using RIE (reactive ion etching), so that oxide is left adjacent to the vertical walls. The net effect of the sidewall spacers and lightly doped drain is an improvement in the hot electron degradation by a reduction of the electric field.

Following the source-drain implants, the interlevel oxide dielectric is deposited. The contacts are made by RIE etching down to the silicon. After the resist is removed, the wafers are RIE etched again to clean the bottom of the contacts. Before this procedure was used, the bottom of the contacts was cleaned with a wet etch, with poor reliability. Molybdenum is used as the first layer of metallization because of its resistance to electromigration and because it makes good ohmic contact to N+ silicon.

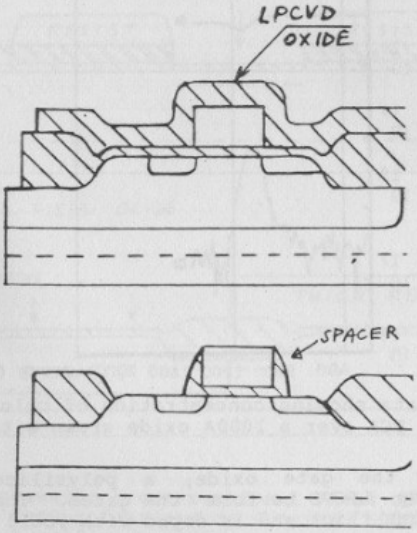

Fig. 3. Cross-sectional view of the A/VLSI process during fabrication showing the LPCVD conformal oxide grown over the the gate and then etched by RIE to form gate oxide spacers.

The second dielectric is a thick oxide layer which is planarized by spinning a resist layer over it and reflowing it with a postbake. The planarized surface of the photoresist is transferred to the second dielectric oxide using an RIE etch in which the resist and the oxide etch at the same rate until the resist is entirely removed. This is shown schematically in Fig. 4 The etch rate ratio of photoresist and oxide is shown in Fig. 5 (2) as a function of the ratio of the NF_3 etchant gas to argon. The method depends on this ratio being controlled at unity. This planarization works well at reducing local step height variations for better metallization step coverage (3), but on the wafer scale, the actual planarization level is influenced by the density of steps in a given region. Hence vias down to a given layer may require different vertical distances depending on the local circuit design.

The second metal is aluminum, which is DC magnetron sputtered. The vias are etched with a semitapered process for good step coverage. This is done by two step etching, in which RIE etching with a straight profile is followed by tapered etching. Passivation is done with low temperature deposited oxide and the final step in the process is a low temperature hydrogen anneal.

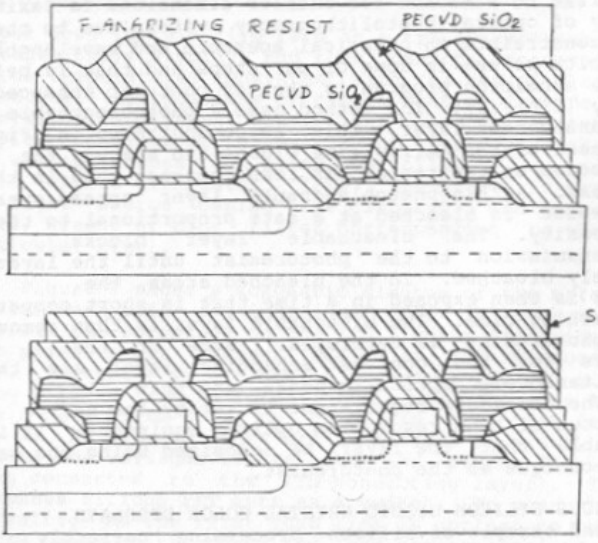

Fig. 4. Cross-sectional view of the A/VLSI process during fabrication showing the second interlevel dielectric and planarizing resist which is etched by RIE to form a planar layer of SiO2.

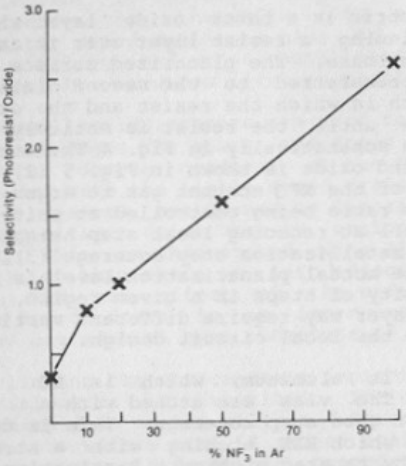

Fig. 5. NF3/Ar composition vs etch rate ratio of resist to silicon dioxide.

The drive to 1 micron and smaller dimensions is taxing the ability of optical photolithography systems due to the practical constraints on numerical aperture and wavelength. A method which we use in some of our steps and that is being used in the submicron program is that of contrast enhanced lithography (CEL) (4). The method uses a photobleachable contrast enhancement layer. This is demonstrated in Fig. 6 (4). Because of the narrow line widths and spaces, the image projected on the resist has less contrast than in the original mask. A thin photobleachable layer spread over the photoresist is bleached at a rate proportional to the photon intensity. The bleachable layer blocks optical transmission to the photoresist until the layer is completely bleached. In the bleached areas, the photoresist is then exposed in a time that is short compared to the bleaching time. The bleachable layer is then removed and the photoresist is developed. Some of the requirements for the contrast enhancing layer are that it be simultaneously optically dense and thin (1 micron). The thickness requirement is set by the narrow depth of focus of high resolution optical equipment. It is also desirable that the layer be deposited using the same spinning technique as the photoresist.

III. AMORPHOUS SILICON LIQUID CRYSTAL COLOR DISPLAYS

A second example of silicon processing currently under intensive investigation at the author's institution as well as in many other locations is that of large area displays using amorphous silicon thin film transistors. It is a beautiful example of the use of amorphous silicon. The application requires a much larger wafer area than is presently available with single crystal silicon, that can

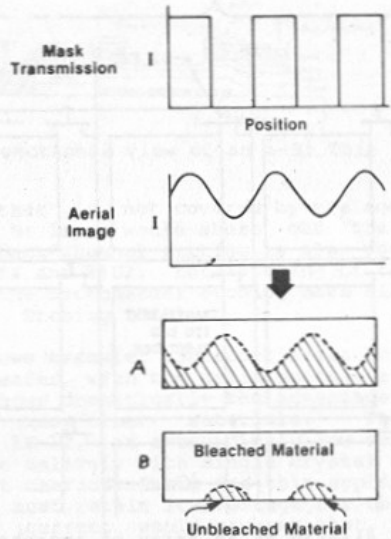

Fig. 6. The aerial image of a high resolution mask bleaches the bleachable layer to replicate the mask on the wafer.

be put down in thin film form on a transparent substrate for a transmissive display, and that can be processed entirely at low temperatures consistent with the use of glass as a substrate. Applications of such a display include television, instrument panels, and computer terminals. The display consists of a matrix of liquid crystal pixels, the voltage across each being controlled by an individual field effect transistor (FET). The light is transmissive (a light source behind the display), and passes through a red, green, or blue filter corresponding to the particular pixel.

Figure 7 shows a schematic diagram of the array of pixels, each with its individual FET in a corner which controls the potential on the ITO (indium tin oxide) layer. Each pixel in our present design is 250 microns on a side. Presently we are making arrays of 160,000 pixels, using a 10 cm X 10 cm format. This will increase to 360,000 pixels on a 15 cm X 15 cm array in the next few months. The X, Y address lines are 10 microns in width, and control the voltages to the gate and source (the drain being connected to the ITO conducting layer). The amorphous silicon FET acts as a switch. To scan the array, the voltage on the first scan line is applied to turn on all of the gates in the first row, and the appropriate voltage is applied to each data line for the desired source potential for each FET. This establishes the voltage of each pixel in the first row. This procedure is sequenced for the entire array, row by row, and can be repeated at television repetition rates.

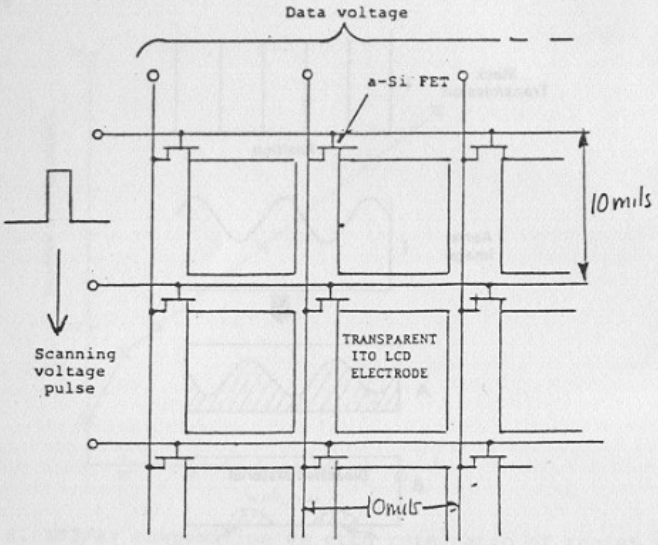

Fig. 7. Schematic diagram of an array of amorphous silicon FETs controlling the potential of the ITO pixel area.

The ITO area comprises about 80% of the wafers area, the remaining 20% being taken up by the FETs and the scan and data lines. Another glass plate with a continuous conducting ITO layer is spaced 6 microns apart from the glass plate with the matrix FET array. Both ITO layers are coated with an alignment layer for the liquid crystal, and the space between the two layers are filled with a twisted nematic liquid crystal.

Figure 8 shows a diagram of a cross section of an amorphous silicon FET fabricated using our process. The gate material (titanium) is deposited directly on the glass surface. (We deposit an SiO2 layer by PECVD first on the glass). Then a "sandwich" of SiN, amorphous Si, and N+ a-silicon is deposited in succession in a PECVD reactor in a single pumpdown. The SiN is the gate insulator, and the N+ is formed admitting phosphene to the silane and argon mixture. The N+ assists in making good contact to the source and drain. The ITO is then deposited by sputtering, and this is followed by sputtering the source and drain metal (molybdenum). The entire process is simple, with four masking steps (gate, silicon "sandwich", ITO, and source/drain). The silicon etching is done in a barrel reactor using CF4 and 8% oxygen. The titanium is also etched in a barrel reactor using CF4 and 8% oxygen. The ITO is presently done using a liftoff process, and the moly is etched using a wet PAWN etch (phosphoric, acetic, water and nitric acids). After patterning the source and drain, the array must be etched to remove the

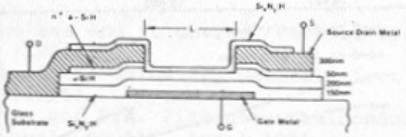

Fig. 8. Cross-sectional view of an a-Si Thin Film Field Effect Transistor.

N+ silicon that is not covered by the source and drain. Otherwise the N+ layer would short out the source and drain. This back-channel etching is also done in a barrel etcher with CF4 and 8%02. Both etching of the silicon sandwich and the backchannel etching have also been done by Reactive Ion Etching (RIE).

Fig 9 shows transfer characteristics for several FETs on the same wafer, with the drain voltage at 10 volts. This figure shows dramatically the advantage of amorphous silicon over many other materials. The off current is commonly 1E-12, an astoundingly low value. Such a low value would be unlikely with single crystal silicon. It is a very important characteristic for this application, because the ITO pixel must retain its voltage for the refresh time, and a leakage current would prevent that. Other workers occasionally build in a capacitor for each pixel element so that a larger leakage current can be tolerated. This of course necessitates a larger charging current as well.

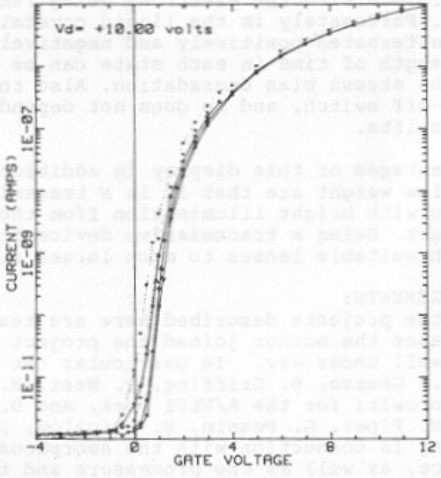

Fig. 9. Drain current versus gate voltage at a drain voltage of 10V for several FETs on the same wafer.

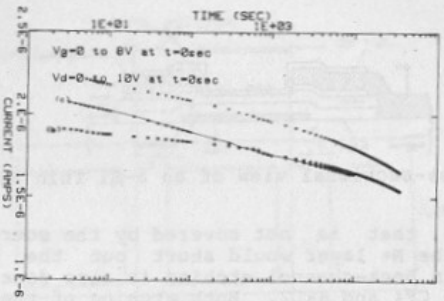

Fig. 10. Stress bias degradation of the drain current in the ON state (see text).

A stringent long-term stability test for amorphous silicon FETs is the static voltage bias test. In a liquid crystal display, the voltages are alternated between positive and negative, as required by the liquid crystal. However if we operate the FET in a DC mode, we get a threshold shift that increases with time, as is illustrated in Fig.10 (5). Here curve a was obtained with the grid held at +8V and the drain at +10 volts. The drain current decays logarithmically by about 20% corresponding to a shift in threshold voltage. If we put a negative voltage on the gate and then repeat the sequence, curves b and c were obtained. The shift is believed to be due to hot electrons that are trapped in the silicon nitride gate insulator. Most of the shift is reversible with the electrons being removed from the insulator. Fortunately in the liquid crystal display the voltages are alternated positively and negatively each cycle so, and the length of time in each state can be controlled to minimize the stress bias degradation. Also the FET acts only as an on-off switch, and so does not depend critically on threshold shifts.

Some advantages of this display in addition to its thinness and low weight are that it is a transmissive device, and so with bright illumination ffom the rear can be extremely bright. Being a transmissive device it can also be projected with suitable lenses to much larger sizes.

IV. ACKNOWLEDGEMENTS:

Both of the projects described here are team efforts, and in both cases the author joined the project when the efforts were well under way. In particular the author is indebted to M. Ghezzo, B. Griffing, P. West, R. Wilson, R. Saia and B. Gorowitz for the A/VLSI work, and D. Castleberry, W. Piper, G. Possin, E. Bigelow, J.Kingsley, and B. Griffing in connection with the amorphous silicon display project, as well as the processors and technicians who did much of the work.

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